REMARKS

The present reply is responsive to the final Office Action dated January 12, 2005. No claims have been amended. New claims 35-37 have been added. No new matter has been introduced in the new claims. Claims 1-37 are presented for the Examiner's consideration in view of the following comments.

As an initial matter, the previous Office Action dated July 14, 2004 objected to the abstract, the title, and the drawings. These objections were addressed in the previous response dated October 14, 2004. However, the current Office Action does not address these objections at all.

In the previous response, a new abstract was submitted to remove the file identifier on the page. As the original drawings were objected to under 37 C.F.R. § 1.83(a), additional drawings were submitted to expressly illustrate all of the features of the claimed invention. As stated in the previous response, no new matter was added by the new drawings, as the features of the supplemental drawings are fully supported by the original claims and specification as filed. Moreover, the drawings illustrate examples of the claims, and should not be deemed to limit the scope of the claims.

Finally, in the previous response applicant respectfully disagreed that the title is not descriptive. The title of the instant application is "System and Method for Processing Complex Computer Instructions." As described in the background of the invention, "[c]omputers routinely perform complex tasks by breaking a single, complex task into a series of simpler instructions that the computer understands." (Specification ¶ 0001.) Aspects of the claimed invention are directed to "a system and method which is capable of quickly emulating complex instructions." (*Id.*, ¶ 0006.) Furthermore, independent claim 1 recites "[a] system for processing a

computer instruction from a source of such instructions," which includes "a complex instruction detector." Independent claim 15 recites "[a] method of processing a computer instruction comprising" including "determining whether the computer instruction is complex." Therefore, applicant respectfully requests that the aforementioned objections to the abstract, drawings, and title be withdrawn.

The Examiner rejected claims 1-2, 4-5, 9-11, 23, and 26-30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,781,750 to *Blomgren et al.* ("*Blomgren*"). Applicant respectfully traverses the rejection.

As discussed in the previous response, *Blomgren* teaches a CPU for handling two distinct instruction sets, CISC and RISC. When an extended RISC instruction is present, the system enters an emulation mode, wherein "complex instructions can be detected by the hardware and trapped to a software emulation driver. Thus some of the complexity of the CISC architecture is moved to the software driver. However, the emulation driver must be isolated and hidden from the user's code being executed; otherwise the user programs could modify or destroy the emulation code, resulting in a system crash." (Col. 5, lns. 17-23.) When in emulation mode, "[a] software routine will be executed that breaks the complex CISC instruction down into several smaller RISC instructions." (*Id.*, lns. 58-61.)

A mode register "contains bits to indicate the current operating mode of the CPU. One bit selects between the RISC and CISC user modes, while another bit enables the extended RISC instructions for emulation mode." (Col. 6, lns. 28-32.) Extended emulation mode instructions "are enabled by enable block 44, which is controlled by the emulation mode bit in the mode register 38." (*Id.*, lns. 52-53.) A multiplexer "selects

the decode instruction from either the RISC or the CISC decode sub-block. Mux 46 is controlled by the RISC/CISC mode control bit in mode register 38." (*Id.*, lns. 53-56.)

Independent claims 1, 23 and 26 each require determining whether an instruction is a member of a set of instructions (*e.g.*, a member of a set of complex instructions). Claim 1 recites "the output being indicative of whether the instruction is a member of a set of instructions." Claim 23 recites "determining whether the original instruction is a member of the set of instructions." Claim 26 recites "output a value indicative of whether the instruction is a member of a set of instructions." Furthermore, claim 26 has been amended to recite "an address generator connected to the memory so as to receive computer instructions from the memory and to generate an address" in order to provide antecedent basis support for the term "address."

If a determination is made that the instruction is a member, then an address is extracted and a jump instruction executed. If a determination is made that the instruction is not a member, then another type of instruction is chosen. For example, claim 1 recites "the output comprising either the instruction from the source or the instruction from the jump instruction generator depending upon the output of the complex instruction detector." Claim 23 recites "selecting the jump and link instruction or the original instruction based on the result of the step of determining." Similarly, claim 26 recites "whereby depending on the value from the complex instruction detector, either the jump instruction or the computer instruction is provided by the instruction selector to the processor."

In each of these independent claims, a selection is made between an "original" instruction (*e.g.*, the instruction

from the source in claim 1, the original instruction in claim 23, or the computer instruction in claim 26) and a "jump" instruction (*e.g.*, the instruction from the jump instruction generator of claim 1, the jump and link instruction of claim 23, or the jump instruction of claim 26). The "jump" instruction is generated based at least in part on the "original" instruction.

In contrast, the multiplexer of *Blomgren* simply determines whether the CPU is operating in a RISC mode or a CISC mode without regard to whether the instruction is a member. The multiplexer does not select a jump instruction based on whether the newly-loaded instruction is a member but rather based on the value of a bit flag common to the entire chip and without regard to whether any individual instruction is complex or not.

Blomgren does not teach or suggest whether the bit flag value is based upon the instruction undergoing processing. According to the Office Action, *Blomgren* "determines whether the next instruction is a member of the RISC set of instructions or a member of the CISC set of instructions based on the mode bits." (Office Action, numbered paragraph 44, pg. 13.) Accordingly, *Blomgren* is not selecting jump instructions based on whether an instruction is a member of a set of instructions, but rather based on a bit flag set by a programmer or the like.

Blomgren neither teaches nor suggests determining whether an instruction is a member of a set of instructions and selecting between an "original" instruction and a "jump" instruction based upon the determination.

According to the Office Action, the "jump instruction generator" is found in *Blomgren* at col. 7, lns. 36-42. This section states:

> When entry to emulation mode is requested, entry point block 56 generate the proper entry point vector or address in the emulation portion of

> memory, and loads this address into the instruction pointer 34. Thus the CPU will begin fetching and executing instructions at the specified entry point, where the emulation driver contains a routine to handle the exception.

In contrast, in the independent claims at issue, the "jump" instruction is generated based at least in part on the "original" instruction. There is no such teaching in *Blomgren*. Therefore, for at least these reasons, *Blomgren* lacks a disclosure or teaching of all of the elements of independent claims 1, 23 and 26. Thus, applicant respectfully requests reconsideration and allowance of these claims. Claims 2, 4-5, 9-11 and 27-30 depend from claims 1 and 26, respectively, and contain all of the limitations thereof as well as other limitations that are neither disclosed nor suggested by the prior art of record. Accordingly, applicant submits that the dependent claims are likewise patentable.

New independent claims 35-37 each require that a determination be made as to whether the instruction at issue "is a complex instruction on an instruction by instruction basis." There is simply no such teaching or suggestion in *Blomgren* for this requirement. In fact, it appears that *Blomgren* teaches away from such a requirement, because, as discussed above, future instructions appear to be selectively processed in *Blomgren* based upon a predetermined value in the bit flag.

Claims 15-22, 31, and 33-34 were rejected under 35 U.S.C. § 103(a) as being obvious over *Blomgren* in view of "Computer Architecture A Quantitative Approach," by Hennessy & Patterson (hereinafter "*Hennessy*"). Applicant respectfully traverses the rejection.

Claims 15-22, 31, and 33-34 deal with performing complex computer instructions in parallel with address generation and jump instruction generation. Specifically,

independent claim 15 requires "wherein determining whether the computer instruction is complex is performed in parallel with the steps of generating the address and generating the jump instruction." Similarly, independent claim 31 requires "wherein the complex instruction detector operates in parallel with the address generator and the jump instruction generator."

Applicant respectfully submits that *Blomgren* and *Hennessy*, taken alone or in combination, neither disclose nor suggest the parallel process of either claim 15 or of claim 31. Indeed, as will be demonstrated below, the Examiner's rejection should be withdrawn for two reasons: (1) the combination does not result in the claimed invention; and (2) there is no motivation to combine the references to arrive at the invention.

As to the first requirement, the technical teachings of *Blomgren* and *Hennessy* are such that their combination would not result in the claimed invention. As stated in the previous response, *Blomgren* neither teaches nor suggests the parallel process of either claim 15 or of claim 31. An attempt was made in the Office Action to remedy this substantial deficiency by relying on Hennessy. According to the Office Action:

> *Blomgren et al.* have not specifically taught wherein determining whether the computer instruction is complex is performed in parallel with the steps of generating the address and generating the jump instruction. However, *Hennessy* has taught that increasing parallelism increases the overall performance and instruction throughput of the system.
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> (Office Action, numbered paragraph 18, pg. 6.)

Hennessy is directed to instruction-level parallelism in a pipeline processing system. The section of *Hennessy* provided to applicant by the Examiner and relied on in the rejection merely lists a variety of pipelining techniques to extend "the pipelining ideas by increasing the amount of

parallelism exploited among instructions." (*Hennessy*, § 4.1.) In particular, "The amount of parallelism available within a basic block (a straight-line code sequence with no branches) ...is quite small...Since these instructions are likely to depend upon one another, the amount of overlap we can exploit within a basic block is likely to be much less than six. To obtain substantial performance enhancements, we must exploit ILP [instruction-level parallelism] across multiple basic blocks." (*Id.*, pgs. 222-23.) The Examiner relies on this teaching in an attempt to reengineer the architecture of *Blomgren* to perform parallel processing in the manner required by independent claims 15 and 31.

The parallel pipelining discussed in *Hennessy* only teaches how to pipeline across multiple straight-line code sequence with no branches. It does not teach or suggest processing jump instructions or selecting between a jump instruction and a complex computer instruction. Thus, *Hennessy* cannot remedy the deficiencies of *Blomgren*.

Even if one could import the teachings of *Hennessy* into *Blomgren*, which applicant does not believe is the case, the combination would not have each and every element required by independent claims 15 and 31. Instead, at best, the processing architecture of *Blomgren* would be capable of pipelining across multiple straight-line code sequence with no branches. Also, there is no teaching or suggestion as to how *Blomgren* could be redesigned to incorporate the "instruction-level parallelism" of *Hennessy*. Finally, it is not even clear that such a combination is feasible in a system structured to handle incompatible RISC and CISC instructions.

As to the second requirement, for the Examiner to meet her burden under 35 U.S.C. § 103(a) to reject, for example, claim 1, she must establish that one skilled in the art would be

motivated to combine the teachings of *Blomgren* and *Hennessy*. Neither reference provides such motivation. As acknowledged in the Office Action, *Blomgren* does not teach the parallel processes required by claims 15 and 31. As stated above, one would have to physically alter the processing system of *Blomgren* to enable parallel processing. The fact that a prior art process or device could be modified so as to produce the claimed invention is not a basis for an obviousness rejection unless the prior art suggests the desirability of such modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). As stated in *In re Oetiker*, 997 F.2d 1443, 1447, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992):

> There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge cannot come from the applicant's invention itself.

There is simply no teaching or motivation in the cited art to rebuild the *Blomgren* system using the "instruction-level parallelism" of *Hennessy* in order to arrive at the parallel process of complex instruction determination and jump instruction generation required by either claim 15 or 31.

In view of the foregoing, it is respectfully submitted that independent claims 15 and 31 patentably distinguishes over *Blomgren* and *Hennessy*, both individually and in the combination, albeit improper, that the Examiner suggests can be made therefrom. Therefore, applicant respectfully requests reconsideration and allowance of these claims. Claims 16-22 and 33-34 depend from claims 15 and 31, respectively, and contain all of the limitations thereof as well as other limitations that are neither disclosed nor suggested by the prior art of record. Accordingly, applicant submits that the dependent claims are likewise patentable.

Claims 6-8 and 12-14 were rejected under 35 U.S.C. § 103(a) as being obvious in view of *Blomgren*. Claims 3, 24-25 and 32 were rejected under 35 U.S.C. § 103(a) as being obvious over *Blomgren* in view of U.S. Patent No. 5,826,089 to *Ireton* ("*Ireton*"). Claim 32 was rejected as being obvious over *Blomgren* in view of *Ireton*. For at least the reasons discussed above, independent claims 1, 15, 23, 26, 31, and 35-37 are patentable. Claims 3, 6-8, 12-14, 24-25 and 32 depend from independent claims 1, 23 and 31, respectively, and contain all of the limitations thereof as well as other limitations that are neither disclosed nor suggested by the prior art of record. Accordingly, applicant submits that the dependent claims are likewise patentable.

As it is believed that all of the objections and rejections set forth in the Official Action have been fully met by the foregoing amendments and remarks, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which she might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By 

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